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Reverse-blocking modular multilevel converter for battery energy storage systems

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Abstract Energy storage systems with multilevel converters play an important role in modern electric power systems with large-scale renewable energy integration. This paper proposes a reverse-blocking modular multilevel converter for a battery energy storage system (RB-MMC-BESS). Besides integrating distributed low-voltage batteries to medium or high voltage grids, with the inherited advantages of traditional MMCs, the RB-MMC-BESS also provides improved DC fault handling capability. This paper analyzes such a new converter configuration and its operating principles. Control algorithms are developed for AC side power control and the balancing of battery state of charge. The blocking mechanism to manage a DC pole-to-pole fault analyzed in depth. Comprehensive simulation results validate both the feasibility of the RB-MMC-BESS topology and the effectiveness of the control and fault handling strategies.

Keywords Reverse blocking, Modular multilevel converter, Battery energy storage system, SOC control, Fault blocking

1 Introduction

In recent years, ever-increasing energy demands and shortage of traditional fossil fuels seriously challenged the sustainable development of human society. At the same time, increasing concern about environment problems and carbon emissions of fossil fuels has provoked worldwide active research on the next-generation electric power system, which is known as the smart grid [1–3] and/or energy internet (EI) [4, 5]. It features renewable energy resources and intelligent energy management. The coming energy power generation system shifts from reliance on fossil fuels to various renewable energy resources, such as solar and wind power, etc. [6] However, the stochastic nature of some renewable resources also brings new challenges to the reliability and stability of existing power grids. Thus it is expected that using grid-connected energy storage system (ESS) for power buffering, peak shaving, load levelling and load frequency control, shall be important for modern electric power systems with large-scale renewable energy integration [7, 8]. Available energy storage technologies include batteries, super capacitors, flywheels, and pumped hydro storage, where batteries are generally

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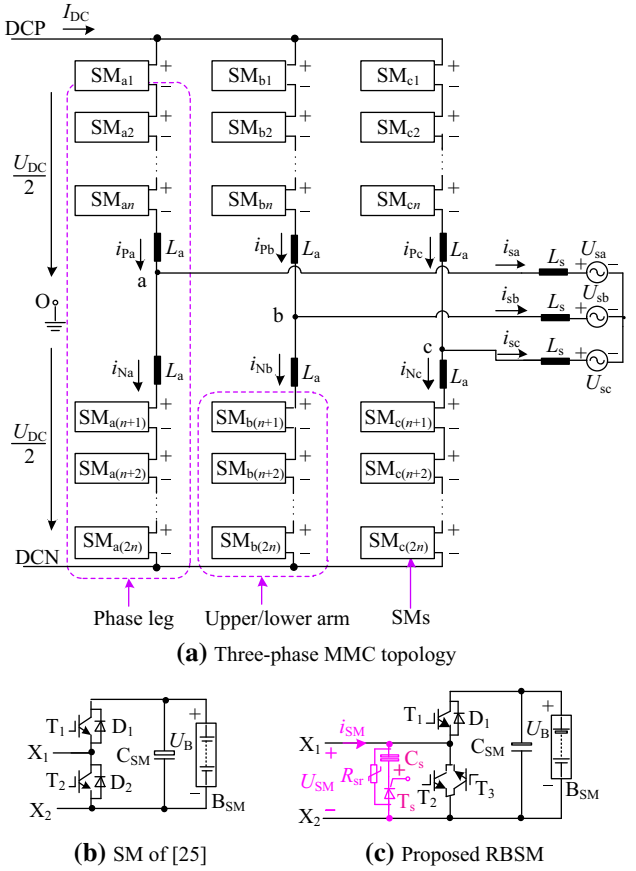
considered as the dominant new solution for large-scale ESS due to its ability to supply power for periods of up to a few hours [9, 10]. The cost of batteries is descending rapidly and is expected to compete with pumped hydro in the near future [11].

To integrate battery energy storage system (BESS) installations to the grid, power converters should have the following features: (1) fault ride-through capability; (2) high redundancy and error correction capabilities. For megawatt-scale medium-voltage (MV) application, multilevel converters show significant advantages over conventional topologies [12]. Among them, the most promising concept for renewable energy integration and power transmission is the modular multilevel converter (MMC) [13–15]. Compared with conventional multilevel converters, MMCs provide advantages of high modularity, better harmonic spectra, lower switching frequency, higher efficiency, and reduced weight of the filtering components.

In the last decades, MMCs have attracted the interest of both academia and industry. The published literature mainly relates to their applications to high-voltage DC (HVDC) transmission [16–18], MV electric drives [19–21], and STATCOMs [22, 23]. MMCs used in BESSs for interfacing low- or medium-voltage batteries to medium- or high-voltage grids were reported in [24–27]. They enable a flexible scaling of power modules to integrate energy storage and power electronics to a wide range of operating voltages, output power and stored energy. However, existing MMC-based BESSs (MMC-BESSs) do not address DC fault handling capabilities, and special control issues arising in MMC-BESSs have not yet been fully overcome. Reverse blocking (RB) IGBTs have a symmetrical blocking voltage characteristic. Due to cancelling anti-parallel diodes, the conduction loss of RB-IGBTs is lower than that of normal IGBTs, so they are especially suitable for multilevel converters for low switching frequency application [28].

This paper proposes a reverse blocking MMC-BESS (RB-MMC-BESS) for enhancing the DC fault handling capability, which consists of new sub-modules (SMs) and distributed battery banks. Typical operating principles, detailed battery energy controls, and fault blocking mechanisms are thoroughly analyzed.

The paper is organized as follows. Section 2 describes the configuration and operating principles of RB-MMC-BESSs. Section 3 explores the battery energy and state of charge (SOC) balancing controls in detail. The DC fault blocking mechanism is analyzed in Section 4. To validate the feasibility and effectiveness of the proposed topology and theoretical analysis, extensive simulation results are discussed in Section 5. Finally, Section 6 reports the main conclusions.



(a) Three-phase MMC topology

(b) SM of [25]

(c) Proposed RBSM

Fig. 1 General configuration of three-phase MMC-BESS

2 Topologies and basic operations

2.1 Topologies for RB-MMC-based BESSs

A typical $(n+1)$ level three-phase MMC-based BESS is shown in Fig. 1, comprised of three phase legs where each leg contains a stack of $2n$ identical sub-modules (SMs) and two inductors (L_a).

For the convenience of discussion, the phase legs are further divided into an upper arm and a lower arm. Unlike conventional MMCs, the SMs integrate a battery storage bank B_{SM}, which can also serve as an active power port. Fig. 1b illustrates one of the possible SM realizations proposed in [25], which consists of two IGBTs with antiparallel diodes and one capacitor that together form a typical bidirectional chopper. The distributed battery banks are directly connected across the SM capacitors. However, when a common DC link short-circuit fault happens, the diode D_2 in each SM will create a fault current path. Large fault currents cause thermal overstress, which may result in severe damage to power electronic devices.

The proposed reverse blocking sub-module (RBSM) is illustrated in Fig. 1c. Unlike the abovementioned SM, two anti-parallel RB-IGBTs (T_2 and T_3) are used for the lower

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switch, and a bypass circuit consisting of auxiliary thyristor T_S, auxiliary capacitor C_S and varistor R_{sr} is connected in parallel with the RB-IGBTs. The distributed battery banks are directly connected across the RBSM capacitors C_{SM} as before. A MMC-BESS employing RBSMs is hereafter called a RB-MMC-BESS.

Due to their high degree of modularity, RB-MMC-BESSs employ distributed battery banks with lower voltage ratings rather than centralized ones used with a conventional high-voltage common DC link. In case of battery faults, extra RBSMs can be placed in the phase leg to replace the damaged ones. RB-MMC-BESSs also have a fixed common DC link, which may be used to interconnect them with a MV DC network if desired. What is more, RB-MMC-BESSs may also transfer power from one phase leg to another using the controlled internal circulating current through this common DC link. This is the theoretical basis for SOC balancing control among phase legs.

2.2 Operating principles of RBSMs

Under normal operations, T_2 and T_1 operate with complementary switching states, while T_3 is switched on all the time and acts as a free-wheeling diode. Once fault current is detected, the RBSMs go into fault protection mode by blocking the control signals of the IGBTs (T_1, T_2 and T_3). Then the fault current starts to charge C_S through T_S, while R_{sr} is designed to prevent over-voltage across C_S, thus it further avoids the potential threats to the main switching devices.

Generally, R_{sr} is not activated until the voltage of C_S exceeds its threshold value. Thus the function of R_{sr} will not be considered in the following to simplify the analysis, but this does not affect the correctness of the theory. The switching states of the RBSM are listed in Table 1, where U_B is the battery voltage of B_{SM} and U_{clamp} is the clamp voltage across T_2 and T_3.

2.3 Operation principles of RB-MMC-BESS

As in [29] and without loss of generality, the following analysis assumes that the operating principles of the three phases are identical, and the conclusions are taken to apply to three-phase conditions. Phase-j is taken as an example to carry out the analysis, where j = a, b, c, and the following additional assumptions are made:

1) Three-phase AC voltages and currents are pure sinusoidal and symmetrical.
2) The common DC link voltage U_{DC} is smooth.
3) The AC output current i_{sj} is distributed equally between the upper and the lower legs.
4) Switching losses of the power devices are ignored.

These conditions are not exact for RB-MMC-BESSs but in general they are fulfilled to a good approximation. The AC terminals of an RB-MMC-BESS are connected to the grid U_{sj} through a series connected filter L_s. With reference direction shown in Fig. 1, the AC currents in normal operating mode are related by:

$$i_{Pj} = \frac{1}{2} i_{sj} + i_{Zj} \tag{1}$$

$$i_{Nj} = -\frac{1}{2} i_{sj} + i_{Zj} \tag{2}$$

$$i_{sj} = i_{Pj} - i_{Nj} \tag{3}$$

$$i_{Zj} = \frac{1}{2}\left(i_{Pj} + i_{Nj}\right) \tag{4}$$

where i_{Pj} and i_{Nj} denote the upper and lower arm currents, respectively. The arm currents flowing through both the upper and lower arms consist of half of the AC output current i_{sj} and the common-mode circulating current i_{Zj}. The role of the latter in balancing the SOC of batteries is discussed below in Section 3.2.

The resulting AC and DC voltages can be calculated as follows :

$$u_{Pj} = \frac{U_{DC}}{2} - u_j - L_a \frac{\mathrm{d}i_{Pj}}{\mathrm{d}t} - R_a i_{Pj} \tag{5}$$

$$u_{Nj} = \frac{U_{DC}}{2} + u_j - L_a \frac{\mathrm{d}i_{Nj}}{\mathrm{d}t} - R_a i_{Nj} \tag{6}$$

$$u_j = \frac{u_{Nj} - u_{Pj}}{2} - \frac{L_a}{2}\frac{\mathrm{d}i_{sj}}{\mathrm{d}t} - \frac{R_a}{2} i_{sj} \tag{7}$$

$$U_{DC} = u_{Pj} + u_{Nj} + 2L_a \frac{\mathrm{d}i_{Zj}}{\mathrm{d}t} + 2R_a i_{Zj} \tag{8}$$

where u_{Pj} and u_{Nj} denote the upper and lower arm voltages, respectively; u_j is the AC output phase voltage; U_{DC} is the rated common DC link voltage; and R_a is the equivalent series arm resistor.

Under a DC link short-circuit fault condition, if the RB-MMC-BESS keeps running according to the above rules before system blocking, U_{DC} will reduce to zero immediately. Then the inserted RBSMs' capacitors C_{SM} and battery banks B_{SM} will be continuously discharged, and potentially over-discharged if the fault is not cleared quickly. Therefore some reasonable means for improving

Table 1 Switching states of a RBSM

Operation modes	State	T_1	T_2	T_3	T_s	i_{SM}	U_{SM}
Normal operation	Discharging	1	0	1	1	<0	U_B
	Charging	0	0	1	1	>0	U_B
	Bypass	0	1	1	1	–	0
Fault protection	Blocking	0	0	0	1	>0	U_B
	Blocking	0	0	0	1	<0	U_{clamp}
System starting	Charging	0/1	0/1	0/1	0	>0	–

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the DC fault ride-through capability of RB-MMC-BESSs should be found.

3 System controls

A RB-MMC-BESS operates differently to a regular MMC. Since each RBSM includes its own battery energy storage, which may act as the DC source, the power is not only delivered from the common DC link. As previously described, each arm conducts only half of the AC output current, thus reducing conduction loss in the converter. Unbalanced SOC of battery banks may cause premature failure after extended cycling due to overcharging or undercharging of batteries. The flat relationship of battery SOC as a function of their voltage, over a wide range of voltages, indicates the need for a SOC balancing algorithm that does not rely on the voltages [30, 31]. Thus SOC control in RB-MMC-BESSs is one of the main differences compared to conventional MMCs.

The controller of a RB-MMC-BESS has two main sections: the power control and SOC balancing control. Fig. 2 shows a block diagram of the system control structure.

3.1 Power control

Active and reactive power control of three-phase RB-MMC-BESSs is based on decoupled current control. Considering the sinusoidal output currents, proportional integration (PI) controllers K_1 are adopted in a rotating frame synchronized with the output frequency. Fig. 3 shows the power control block diagram for a three-phase RB-MMC-BESS. Here, P^* and Q^* represent the power commands for the instantaneous active and reactive power at the AC side, respectively. The AC side active power P^* causes charging and discharging of the RBSMs' capacitors and battery banks, so the SOC and the DC link voltage are indirectly controlled. Finally, the upper and lower arm voltage references U^*_{Pj} and U^*_{Nj} are determined by the AC side power.

3.2 SOCs balancing control

The inherent circulating current among phases is required to charge the capacitors with the lowest SOC and discharge the ones with the highest SOC. Therefore, it is essential to control the circulating current of the converter to maximize the efficiency of the SOC controls. The SOC control structure of RB-MMC-BESS is illustrated in Fig. 4, where K_2 to K_5 refer to close-loop controllers such as PI controllers. SOC balancing control of the RB-MMC-BESS is divided into individual SM balancing, phase arm balancing, phase leg balancing, and inner circulating current control.

Figure 4a shows the block diagram for individual SOC balancing control; sign() denotes the signum function. This is responsible keeping all RBSMs in the same arm at the average arm SOC (i.e. $\overline{SOC}_{Pj}$, $\overline{SOC}_{Nj}$) using a close-loop controller. The average arm SOC $\overline{SOC}_{Pj}$,$\overline{SOC}_{Nj}$ are given by:

$$\overline{SOC}_{Pj} = \frac{1}{n}\sum_{k=1}^{n} SOC_{jk} \tag{9}$$

$$\overline{SOC}_{Nj} = \frac{1}{n}\sum_{k=n+1}^{2n} SOC_{jk} \tag{10}$$

The arm SOC balancing control forces the SOC difference between the upper and lower arms (i.e. $\overline{SOC}_{Pj}-\overline{SOC}_{Nj}$) to be zero. The leg SOC control is

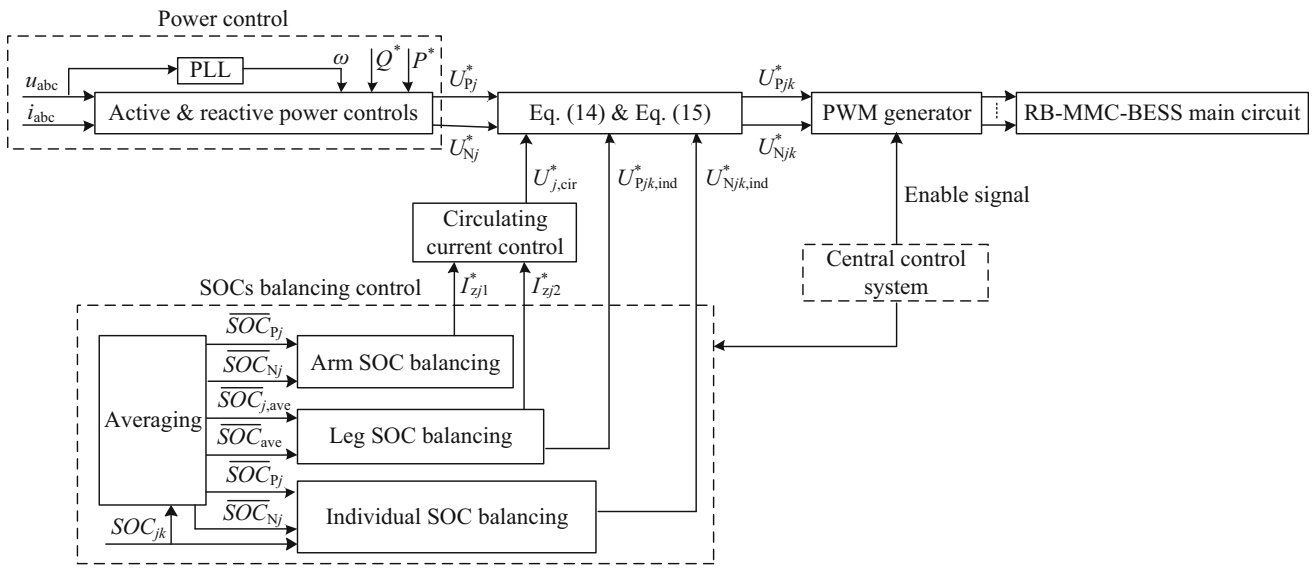

Fig. 2 Overview of system control structures

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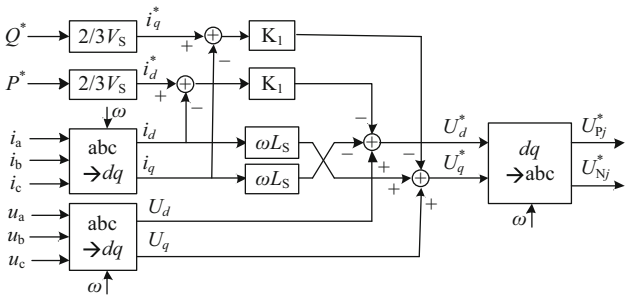
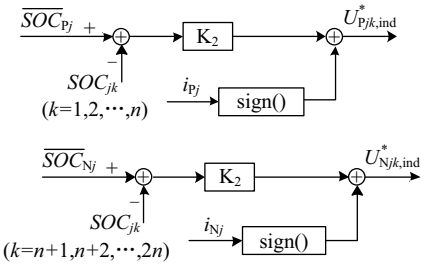
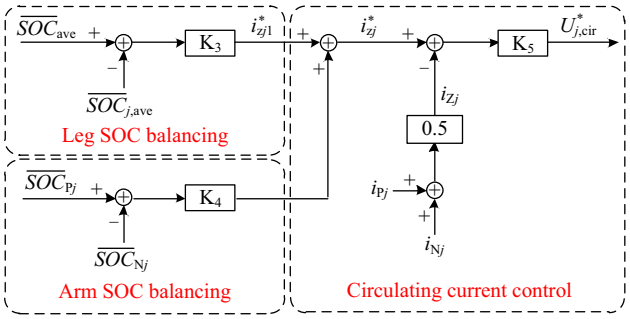


Fig. 3 Block diagram of power control



(a) Individual SOC control



(b) Arm & leg SOC control

Fig. 4 Block diagram of SOC control

designed to force the j-phase average SOC ($\overline{SOC}_{j,\mathrm{ave}}$) to follow the average SOC of the three phases ($\overline{SOC}_{\mathrm{ave}}$), where, $\overline{SOC}_{j,\mathrm{ave}}$ and $\overline{SOC}_{\mathrm{ave}}$ are given by:

$$\overline{SOC}_{j,\mathrm{ave}} = \frac{1}{2n}\sum_{k=1}^{2n} SOC_{jk} \tag{11}$$

$$\overline{SOC}_{\mathrm{ave}} = \frac{1}{3}\sum_{j=a}^{c} \overline{SOC}_{j,\mathrm{ave}} \tag{12}$$

These control objectives can be achieved using the circulating current. Therefore, the output signals of both leg and arm SOC balancing controllers are i^*_{Zj1} and i^*_{Zj2} respectively, from which the reference circulating current i^*_{Zj} is determined:

$$i^*_{Zj} = i^*_{Zj1} + i^*_{Zj2} \tag{13}$$

Together, the arm and leg SOC controls result in direct control of the circulating current in each phase leg, leading to good current regulation of the battery banks. The circulating current control loop is illustrated as Fig. 4. The current minor loop forces i_{zj} to follow the command i^*_{Zj}, which generates the voltage control command $U^*_{j,\mathrm{cir}}$.

Finally, the voltage reference for the upper and lower arm of phase-j is given by:

$$U^*_{\mathrm{P}jk} = \frac{U^*_{\mathrm{P}j}}{n} + U^*_{\mathrm{P}jk,\mathrm{ind}} + U^*_{j,\mathrm{cir}} + \frac{U_{\mathrm{DC}}}{n} \tag{14}$$

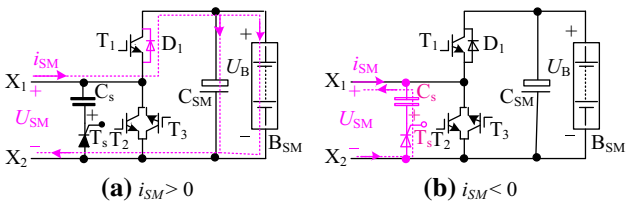
$$U^*_{\mathrm{N}jk} = \frac{U^*_{\mathrm{N}j}}{n} + U^*_{\mathrm{N}jk,\mathrm{ind}} + U^*_{j,\mathrm{cir}} + \frac{U_{\mathrm{DC}}}{n} \tag{15}$$

where the inputs are shown in Fig. 2.

4 DC fault blocking mechanism

A DC pole-to-pole fault is regarded as one of the most serious fault types. Therefore, the theory of the DC fault blocking mechanism will be studied under this condition. Fig. 5 shows the possible current paths after all IGBTs in a RBSM are blocked. When current i_{SM} is positive as shown in Fig. 5a, the capacitor is charged through the anti-parallel diode D_1 and the fault current is limited because the capacitor voltage U_{B} provides an inverse voltage to switch off the diode. Otherwise, when current i_{SM} is negative, the RBSM is bypassed as shown in Fig. 5b. The bypass circuit goes to work and $\mathrm{C_s}$ is charged by the fault current through the triggered $\mathrm{T_S}$. $\mathrm{C_s}$ is generally very small compared with the $\mathrm{C_{SM}}$. Thus u_{cs} will increase quickly to provide the inverse voltage needed to cut off the arc path at the fault point.

Once a pole-to-pole DC short-circuit fault occurs, the common DC link voltage is collapsed to zero and a large inrush current would be induced. Then the RBSMs will enter their discharging stage immediately until system blocking is enabled by the central control system, which is the same behavior as the equivalent model presented in [32]. Rather than repeating the detailed explanation found there, this paper will focus on the fault mechanism in the blocking stage.



(a) $i_{SM}>0$ **(b)** $i_{SM}<0$

Fig. 5 Possible current paths of RBSMs in their blocking state

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4.1 Modelling blocking mechanism

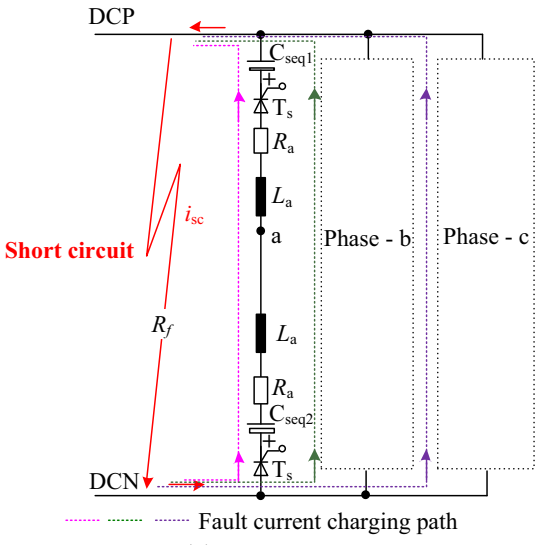
Once the RB-MMC-BESS goes into fault protection mode following a DC pole-to-pole fault, all IGBTs are blocked by the central control system, and the equivalent of a phase leg is illustrated in Fig. 6. The equivalent series capacitance of both the upper and lower arms is expressed as

$$C_{\text{seq1}} = C_{\text{seq2}} = \frac{C_{\text{S}}}{n} \tag{16}$$

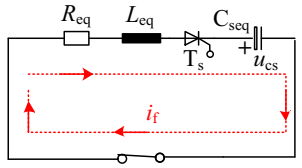
In this state, the fault current starts to charge the auxiliary capacitor C_s through T_s. Then u_{cs} increases quickly to provide the inverse voltage $u_{csI} = 2n \times u_{cs}$,which helps to extinguish the fault current. As shown in Fig. 6b, a second-order oscillating circuit is constructed with the equivalent series resistance R_{eq}, equivalent inductance L_{eq} and the equivalent capacitance C_{seq}. This will govern the discharging of C_{seq} which may be regarded as $2n$ auxiliary capacitors C_s in series. The following differential equation is deduced from Kirchhoff's voltage law:

$$\frac{\mathrm{d}^2 u_{\text{cs}}}{\mathrm{d}t} + \frac{R_{\text{eq}}}{L_{\text{eq}}}\frac{\mathrm{d}u_{\text{cs}}}{\mathrm{d}t} + \frac{1}{L_{\text{eq}} C_{\text{seq}}} u_{\text{cs}} = 0 \tag{17}$$

The initial conditions and circuit parameters are:



(a) Charging loop



(b) Simplified equivalent circuit

Fig. 6 Current path in the RB-MMC-BESS in the blocking state

$$\begin{cases} u_{\text{cs}}(0_+) = u_{\text{cs}}(0_{1-}) = 0 \\ i_{\text{f}}(0_+) = i_{\text{f}}(0_-) = I_0 \end{cases} \tag{18}$$

$$\begin{cases} R_{\text{eq}} = 2R_{\text{a}} + R_{\text{f}} \\ L_{\text{eq}} = 2L_{\text{a}} \\ C_{\text{seq}} = \dfrac{C_{\text{s}}}{2n} \end{cases} \tag{19}$$

where I_0 is defined as the initial fault current at the blocking stage and R_f is the short circuit resistance. Assuming for simplicity that the auxiliary capacitor voltages are equal, then the charging current and voltage of each auxiliary capacitor C_s is:

$$u_{\text{cs}} = e^{-\frac{t}{\tau}} \frac{2nI_0}{\omega C_{\text{s}}} \sin(\omega t) \tag{20}$$

$$i_{\text{f}} = -e^{-\frac{t}{\tau}} \frac{\omega_0 I_0}{\omega} \sin(\omega t - \beta) \tag{21}$$

where τ is the fault current decay time constant, ω_0 and ω are the natural angular frequency and system angular frequency, respectively, and β is the initial current phase angle. These four variables are defined as follows:

$$\begin{cases} \tau = \dfrac{4L_{\text{a}}}{2R_{\text{a}} + R_{\text{f}}} \\ \omega = \sqrt{\dfrac{n}{L_{\text{a}} C_{\text{s}}} - \left(\dfrac{2R_{\text{a}} + R_{\text{f}}}{4L_{\text{a}}}\right)^2} \\ \omega_0 = \sqrt{\dfrac{n}{L_{\text{a}} C_{\text{s}}}} \\ \beta = \arctan \sqrt{\dfrac{16nL_{\text{a}}}{C_{\text{s}}(2R_{\text{a}} + R_{\text{f}})^2} - 1} \end{cases} \tag{22}$$

Equations (20) and (21) indicate that u_{cs} and the fault current i_f are affected by the initial fault current I_0; while u_{cs} is approximately inverse proportional to the RBSM's capacitance. In addition, the fault current i_f is also influenced directly by the equivalent resistance R_{eq} and inductance L_{eq}.

4.2 Selecting parameters of auxiliary circuit

Without considering system redundancy, it is assumed for simplicity that the $2n$ RBSMs are series-connected in each phase leg. The voltage stress of the auxiliary capacitor always equals U_{SM} under normal operating conditions. After system blocking is enabled, the auxiliary capacitors are charged in series by the fault current, and the auxiliary capacitor voltage will reach its peak value as the current decays to zero. From (20), the peak blocking voltage across T_2 and T_3 is

$$U_{\text{clamp}} = \frac{u_{\text{cs,peak}}}{2n} = e^{-\frac{\beta}{\omega\tau}} \frac{I_0}{\omega C_{\text{s}}} \sin(\beta) \tag{23}$$

The voltage stress across C_s is illustrated in Fig. 7, where the clamping voltage is related to both the auxiliary

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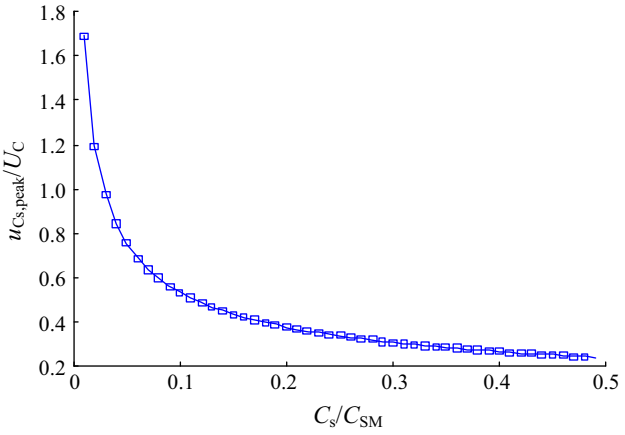

Fig. 7 Voltage stress of C_S in the bypass circuit

capacitance C_s and leg inductance L_a. A larger leg inductance value means that more inductive energy will be transformed to electric field energy, which results in higher capacitor voltage. The smaller the auxiliary capacitance and the larger the initial fault current I_0, the faster the capacitor voltage changes.

Therefore the value of C_s is determined by two parameters: the voltage limit for IGBTs ($U_{T,max}$) and the optimized blocking voltage ($U_{cs,min}$). The latter helps to eliminate the AC rectification feeding energy. Therefore, C_s should satisfy:

$$U_{cs,min} \leq u_{Cs,peak} \leq U_{T,max} \tag{24}$$

4.3 Fault management

Fig. 8 shows the DC fault protection flow chart for the RB-MMC-BESS. The operating state is monitored continuously, with both the DC link voltage and currents sent back to the central control system, so the DC fault state may be judged by comparing them with their threshold values.

Once a DC fault is detected, the system will immediately block all the trigger pulses in the RB-MMC- BESS to clear the fault currents. For non-permanent faults, it is expected that power transmission can be restarted quickly, so the IGBTs will be triggered to test which type of fault has occurred. If the fault is cleared then all the IGBTs are unblocked and the RB-MMC-BESS will be restarted. But if a permanent fault is identified, both the AC breakers and the DC breakers are tripped to achieve fault isolation after fault clearance.

Generally speaking, the fault clearance time achieved by the protection system is very short, perhaps less than 1ms, to protect the main power devices from thermal overstress.

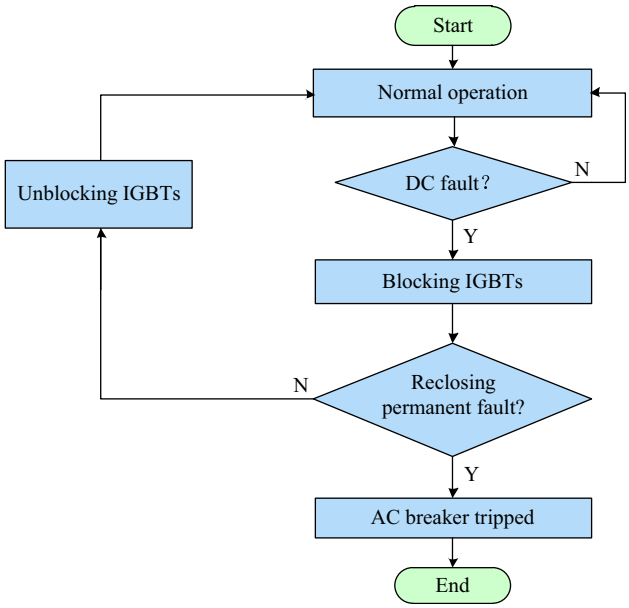

Fig. 8 Flow chart of DC fault protection in the RB-MMC-BESS

5 Verification of RB-MMC-BESS by simulation

To verify the feasibility of the proposed RB-MMC-BESS and system control strategies, a fully switched simulation model has been developed as shown in Fig. 9, where PCC denotes the point of common coupling. The modulation method adopted in this simulation is the carrier phase-shifted sinusoidal pulse-width-modulation methods. Two simulated scenarios are considered in this section. The first simulation focuses on the system control algorithms under normal operating conditions, thus demonstrating control of SOC and power. The second simulation verifies the DC fault handling capabilities of the RB-MMC-BESS under a typical DC pole-to-pole fault.

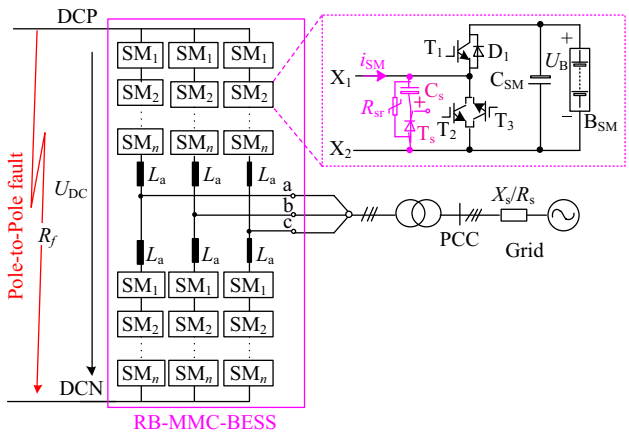

Fig. 9 Diagram of the simulated system

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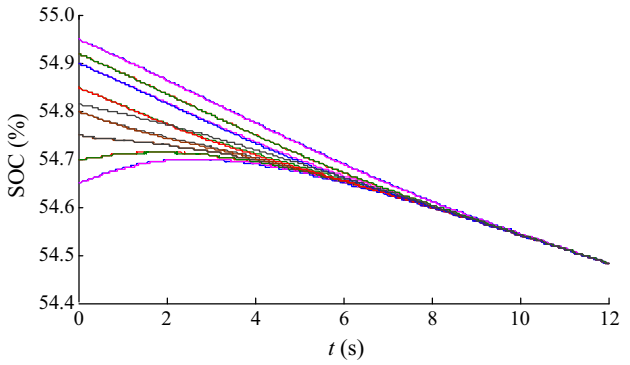
5.1 Scenario 1: RB-MMC-BESS under normal operating conditions

In this scenario, all battery banks in phase a have been initialized with different SOC. After the RB-MMC-BESS starts, the power command $P^* = 2$ MW is issued, and all battery banks in the RBSMs are discharging. The proposed power control and SOC balancing control algorithms have been tested and the results are illustrated in Fig. 10.

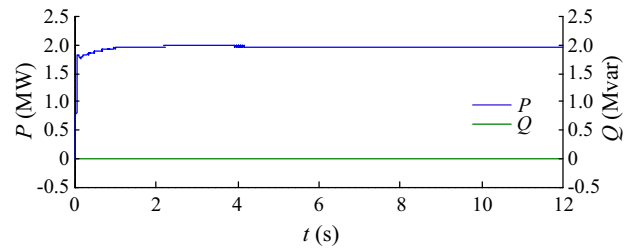
The convergence SOC curves while discharging is shown as Fig. 10a. It is clear that the RBSMs with higher SOC discharge quicker, while some RBSMs with lower SOC are recharged for a period to bring the SOC closer together, before they convert to the same value. With the proposed controller, all the RBSMs' battery banks are completely balanced after 9 s. From the power transmission point of view, the active and reactive power are not affected by the SOC balancing controls, as shown in Fig. 10b. Note that the battery parameters are adjusted to make the simulation time short for this demonstration.

5.2 Scenario 2: RB-MMC-BESS under typical DC fault condition

Since this paper mainly concerns the DC fault handling capability of the proposed topology, simulation of a nine-level RB-MMC-BESS is sufficient to demonstrate the functionality while maintaining simulation efficiency. Table 2 summarizes the simulation parameters. The fault



(a) SOCs of the battery banks



(b) Power transferred

Fig. 10 Convergence of SOC of the simulated battery banks

Table 2 Simulation parameters

System parameters	Value
AC line-to-line voltage	7.2 kV
DC link voltage	16.0 kV
RBSM capacitor voltage	2.0 kV
RBSM capacitance	8.2 mF
Leg inductance	3.5 mH
Short circuit resistance (R_f)	5.0 mΩ
Auxiliary capacitance (C_s)	0.15 μF

scenario is a non-permanent DC pole-to-pole fault scenario that occurs at 0.3 s and is cleared at 0.4 s. The simulation results are shown in Fig. 11 and Fig. 12.

From $t = 0$ s to 0.3 s, the RB-MMC-BESS operates at a power rating of 1 MW, supplied by battery banks in the RBSMs. When the DC pole-to-pole fault occurs at $t = 0.3$ s, the common DC link voltage U_{DC} drops to zero immediately, shown in Fig. 11a. This is accompanied by an inrush DC short current in the fault point, as seen in Fig. 11b. It is further supposed that it takes 0.1 ms to block all the trigger pulses so the RB-MMC-BESS can clear the fault currents. According to the fault blocking mechanism theory in Section 4, the $2n$ series-connected auxiliary capacitor voltages u_{csI} provide the inverse voltage that will help to extinguish the arc fault current in time. Fig. 11c and Fig. 11d illustrate the grid voltages and currents during the DC fault. The short circuit fault energy mainly comes from the DC fault loop shown in Fig. 6. Because the blocking measures are timely, the grid input currents reduce quickly to zero, while the grid voltages are not significantly affected. AC power transmission, shown in Fig. 11e, is interrupted by the DC fault and recovers very quickly after the non-permanent fault is cleared.

Fig. 12 illustrates the performance of RBSMs during the DC pole-to-pole short circuit fault. The SOC and capacitor voltage of each RBSM is shown in Fig. 12a and Fig. 12b. Since all IGBTs are blocked in time, the capacitor voltages remain almost constant at their value at the time of failure, resulting in the constant SOC of the battery banks. This maintains a reasonable condition for restarting the RB-MMC-BESS after the fault is cleared.

Section 3 found that the circulating current can be controlled according to the desired recharge current of the battery banks and the equalizing time. Fig. 12c shows the circulating current during the DC fault. As soon as the RBSMs go into fault protection mode, the fault current i_f transfers to the bypass circuits and starts charging the auxiliary capacitors C_s through T_S. Fig. 12d illustrates the voltage stress of RBSMs. It can be seen that u_{cs} is directly applied to the lower switches T_2 and T_3 when fault protection mode is enabled.

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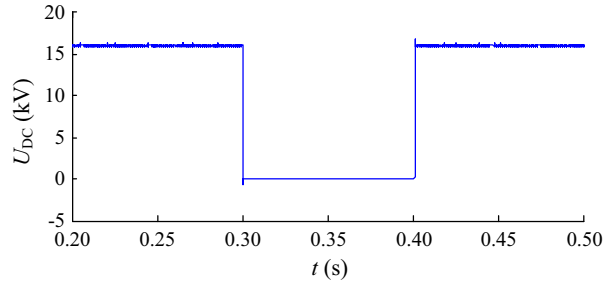
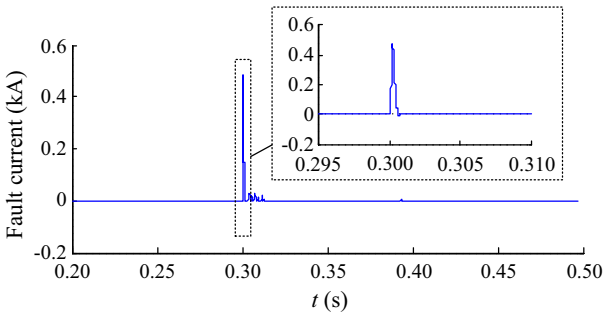
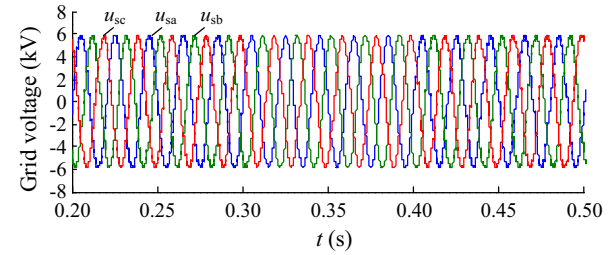


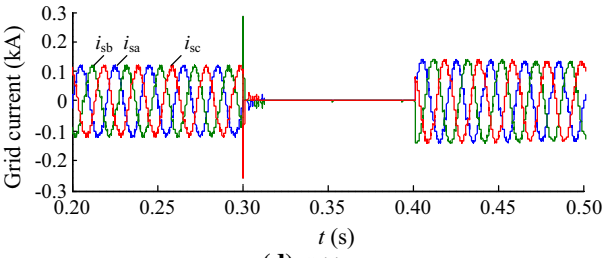
(a) Common DC link voltage



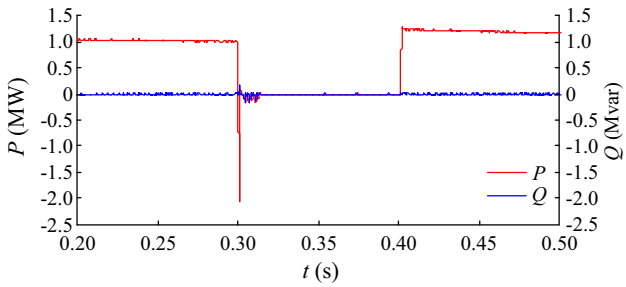
(b) DC fault current



(c) Grid voltage

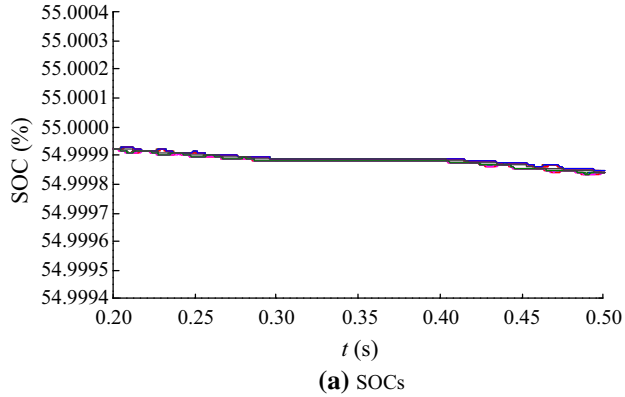


(d) Grid current

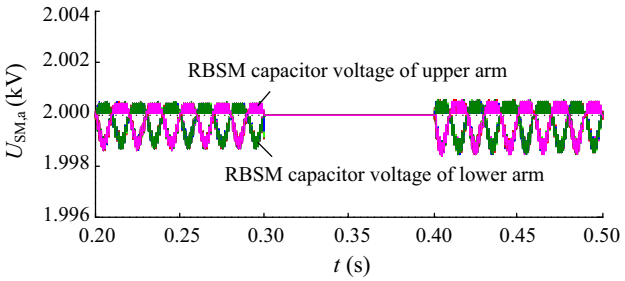


(e) AC power transmission

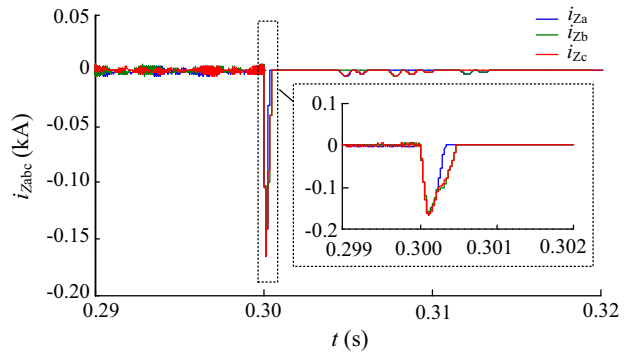
Fig. 11 Simulation results for RB-MMC-BESS during a DC fault



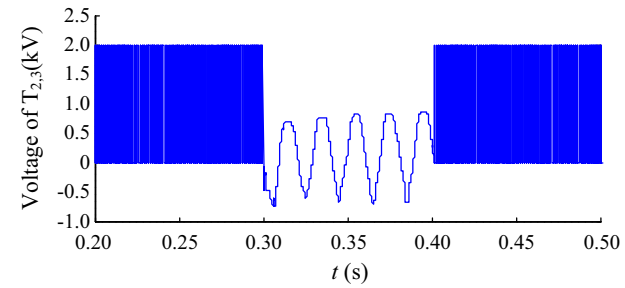
(a) SOCs



(b) Capacitor voltages



(c) Circulating currents



(d) Voltage stress of T_2 and T_3

Fig. 12 Simulation results for RBSMs during a DC fault

Fig. 13 compares the simulated DC fault handling capabilities of a RB-MMC-BESS and a traditional MMC-BESS system. Once DC short circuit fault occurs in the

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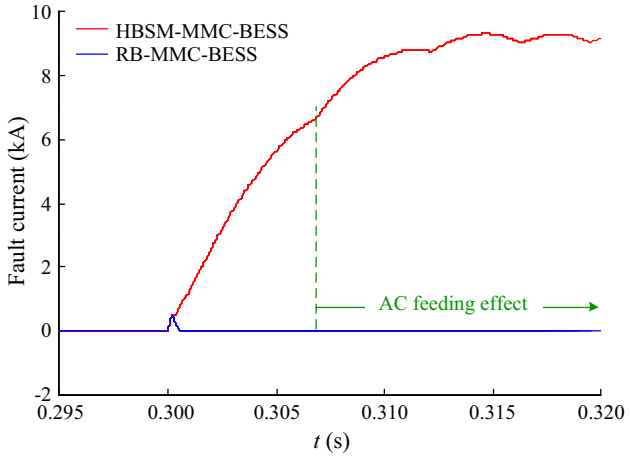

Fig. 13 Fault currents of a RB-MMC-BESS and a traditional MMC-BESS

RB-MMC-BESS and all IGBTs are blocked, the series-connected C_s voltage increases quickly to provide an inverse voltage to suppress the fault current. However, due to the lack of fault current suppression measures, the fault current in the traditional MMC-BESS increases dramatically. The peak value may reach nearly 18 times that of the RB-MMC-BESS under the same conditions. It is evident that the RB-MMC-BESS has better fault blocking capabilities, and this one of its salient merits.

6 Conclusion

This paper has investigated the operation and control of a proposed reverse-blocking modular multilevel converter with a distributed battery energy storage system (RB-MMC-BESS) for interfacing low-voltage batteries to the medium or high voltage grids. Its theoretical performance has been analyzed and the findings have been confirmed through simulation.

Unlike conventional MMC-BESS designs, sub-modules with integrated battery banks use two anti-parallel RB-IGBTs and an additional bypass circuit. The proposed design can block fault currents effectively with reduced requirement for precise trigger pulses during fault conditions. This greatly enhances the ability of the BESS to respond to fault conditions and to ride through non-permanent faults.

The RB-MMC-BESS also employs direct management of state of charge (SOC) of battery banks, rather than sub-module voltages. Control algorithms combining power control and SOC control have been developed and demonstrated through simulation. The standard modulation strategies can be employed under the normal operating condition.

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